WHAT IS CLAIMED IS:

1. A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency; and

an internal clock signal generator for waveform-shaping the external clock signal and generating an internal clock signal depending on the output of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

2. The circuit as claimed in claim 1, wherein the operating frequency decision unit generates a high frequency to determine whether the external clock signal is the high frequency or the low frequency depending on a CAS latency.

3. The circuit as claimed in claim 2, wherein the CAS latency has a value of 0 to 7 and the operating frequency decision unit generates the high frequency if the value of the CAS latency is over 4.

4. The circuit as claimed in claim 2, further comprising a mode register for storing the CAS latency.

5. The circuit as claimed in claim 1, wherein the internal clock signal generator comprises:

a delay unit for delaying the external clock signal by some time; and

a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

6. The circuit as claimed in claim 5, wherein the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

7. The circuit as claimed in claim 5, wherein the pulse-shaping unit comprises:

a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the output of the operating frequency decision unit;

a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted; and

an inverter for inverting the output signal of the second NAND gate.

8. The circuit as claimed in claim 5, wherein the delay unit includes a RC delay circuit.

9. The circuit as claimed in claim 8, wherein the delay unit comprises:

a first inverter for inverting the external clock signal;

a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

10. The circuit as claimed in 9, further comprises:

first fuses connected to both ends of the number of the resistors, respectively, and can be blown; and

second fuses connected to the first nodes and the number of the MOS capacitors, respectively, and can be blown.

11. The circuit as claimed in claim 5, wherein the delay unit comprises:

a first inverter for inverting the external clock signal;

a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

12. The circuit as claimed in 11, further comprises:

first fuses connected to both ends of the number of the resistors, respectively, and can be blown; and

second fuses connected to the first nodes and the number of the MOS capacitors, respectively, and can be blown.

13. The circuit as claimed in claim 1, wherein the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

14. A method of generating an internal clock signal, comprising the steps of:

determining whether an external clock signal is a low frequency or a high frequency; and

waveform-shaping the external clock signal and generating an internal clock signal depending on the result of the determination step, or generating the external clock signal as the internal clock signal as it is.

15. The method as claimed in claim 14, wherein, in the determination step, whether the external clock signal is the high frequency or the low frequency is determined as a CAS latency.

16. The method as claimed in claim 15, wherein the CAS latency has a value of 0 to 7 and the external clock signal is determined as the high frequency if the value of the CAS latency is over 4.

17. The method as claimed in claim 14, wherein the step of generating the clock comprises the steps of:

waveform-shaping the external clock signal and generating the internal clock signal if the external clock signal is the low frequency; and

generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency.